AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (Currently Amended) A pre-stored digital word generator for producing multiple digital words, ~~which~~ wherein the pre-stored digital word generator is applied to trigger a signal generating circuits of a plurality of test channels of a chip tester, the pre-stored digital word generator comprising:

an edge memory used to store a primary preset information;

an edge address counter electrically connected with the edge memory and used to point to an address of the edge memory;

a reloadable down counter electrically connected with the edge memory for accessing the primary preset information of the address that is pointed by the edge address counter, wherein the reloadable down counter counts according to the primary preset information; and

a plurality of word generating circuits electrically connected with the edge memory and the reloadable down counter, further comprising a rise register used to store a first register data of the secondary preset information; a fall register used to store a second register data of the secondary preset information; a rising comparator used to compare the mark_tag data of the primary preset information, which is pointed by the edge address counter, with the first register data to form a rising comparison result; a falling comparator used to compare the mark_tag data of the primary preset information, which is pointed by the edge address counter,

with the second register data to form a falling comparison result; and a latch component used to produce the trigger signals according to the rising comparison result and the falling comparison result;

wherein the word generating circuits having a secondary preset information, wherein the word generating circuits compares the primary and secondary preset information and then produce digital words for triggering the signal generating circuits according to a comparison result;

~~wherein,~~and every time when the reloadable down counter finishes its counting, the reloadable down counter triggers the edge address counter to make the edge address counter point to a next address of the edge memory and trigger the word generating circuits to make the word generating circuits output the digital words.

Claim 2 (Original) The pre-stored digital word generator as claimed in claim 1, wherein the primary preset information comprises a mark_count data, a mark_tag data, a rise_eable data and a fall_enable data.

Claim 3 (Currently Amended) (Currently Amended) [[The]]A pre-stored digital word generator ~~as claimed in claim 3, wherein each of the word generating circuits further comprises:~~

~~a rise register used to store a first register data of the secondary preset information;~~

~~a fall register used to store a second register data of the secondary preset information;~~

~~a rising comparator used to compare the mark_tag data of the primary preset information, which is pointed by the edge address counter, with the first register data to form a rising comparison result;~~

~~a falling comparator used to compare the mark_tag data of the primary preset information, which is pointed by the edge address counter, with the second register data to form a falling comparison result; and~~

~~a latch component used to produce the trigger signals according to the rising comparison result and the falling comparison result;~~ for producing multiple digital words, wherein the pre-stored digital word generator is applied to trigger a signal generating circuits of a plurality of test channels of a chip tester, the pre-stored digital word generator comprising:

an edge memory used to store a primary preset information;

an edge address counter electrically connected with the edge memory and used to point to an address of the edge memory;

a reloadable down counter electrically connected with the edge memory for accessing the primary preset information of the address that is pointed by the edge address counter, wherein the reloadable down counter counts according to the primary preset information; and

a plurality of word generating circuits electrically connected with the edge memory and the reloadable down counter, further comprising a rise register used to store a first register data of the secondary preset information; a fall register used to store a second register data of the secondary preset information; a rising comparator used to compare the mark_tag data of the primary preset information, which is pointed by the edge address counter, with the first register data to form a rising comparison result; a falling comparator used to compare the mark_tag data of the primary preset information, which is pointed by the edge address counter, with the second register data to form a falling comparison result; and a latch component used to produce the trigger signals according to the rising comparison result and the falling comparison result;

wherein the word generating circuits having a secondary preset information, wherein the word generating circuits compares the primary and secondary preset information and then produce digital words for triggering the signal generating circuits according to a comparison result, and every time when the reloadable down counter finishes its counting, the reloadable down counter triggers the edge address counter to make the edge address counter point to a next address of the edge memory and trigger the word generating circuits to make the word generating circuits output the digital words; and

wherein the latch is switched to a high voltage when the mark_tag data of the primary preset information matches with the first register data; the latch is switched to a low voltage when the mark_tag data of the primary preset information matches with the second register data.

Claim 4 (Currently Amended) The pre-stored digital word generator as claimed in claim [[3]]1, wherein the reloadable down counter counts according to the mark_count data of the primary preset information.

Claim 5 (Currently Amended) The pre-stored digital word generator as claimed in claim [[3]]1, wherein the rising comparator is enabled according to the rise_eable data.

Claim 6 (Currently Amended) The pre-stored digital word generator as claimed in claim [[3]]1, wherein the falling comparator is enabled according to the fall_enable data.

Claim 7 (Currently Amended) The pre-stored digital word generator as claimed in claim [[3]]1, wherein the latch component is a flip-flop component.